In the Claims:

1. (Original) A method of generating an integrated circuit netlist, comprising the steps of:

generating a first schematic of an integrated circuit having a plurality of cells therein;

generating a second schematic that defines post-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the post-layout interconnects; and

combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

2. (Original) The method of Claim 1, wherein said step of generating a second schematic comprises the steps of:

generating a layout schematic from the first schematic of the integrated circuit;

generating parasitic resistances and capacitances of the post-layout interconnects that extend between a plurality of cells in the layout schematic; and

generating parasitic resistances and capacitances of interconnects internal to at least one cell in the layout schematic.

3. (Original) The method of Claim 2, wherein said step of combining the first and second schematics comprises combining the first and second schematics into a simulation schematic.

4. (Original) The method of Claim 3, further comprising the steps of:

generating a netlist of at least a portion of the simulation schematic; and

supplementing the netlist with the parasitic resistances and capacitances of interconnects internal to the at least one cell in the layout schematic.

5. (Original) A computer program product that is configured to generate an integrated circuit netlist, comprising a computer-readable storage medium having computer-readable program code embodied in said medium, said computer-readable program code comprising:

computer-readable program code that is configured to generate a first schematic of an integrated circuit having a plurality of cells therein;

computer-readable program code that is configured to generate a second schematic that defines post-layout electrical interconnects between the plurality of cells of the integrated circuit and approximate parasitic resistances and parasitic capacitances of the post-layout interconnects; and

computer-readable program code that is configured to combine the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

6. (Original) The product of Claim 5, wherein said computer-readable program code that is configured to generate a second schematic comprises:

computer-readable program code that is configured to generate a layout schematic from the first schematic of the integrated circuit;

computer-readable program code that is configured to generate parasitic resistances and capacitances of the post-layout interconnects that extend between a plurality of cells in the layout schematic; and

computer-readable program code that is configured to generate parasitic resistances and capacitances of interconnects internal to at least one cell in the layout schematic.

7. (Original) The product of Claim 6, wherein said computer-readable program code that is configured to combine the first and second schematics comprise computer-readable program code that is configured to combine the first and second schematics into a simulation schematic.

8. (Original) The product of Claim 7, further comprising:

computer-readable program code that is configured to generate a netlist of at least a portion of the simulation schematic; and

computer-readable program code that is configured to supplement the netlist with the parasitic resistances and capacitances of interconnects internal to the at least one cell in the layout schematic.

9. (Original) A method of generating an integrated circuit netlist, comprising the steps of:

generating a first schematic of an integrated circuit having a plurality of cells therein;

generating a second schematic that defines pre-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the pre-layout interconnects; and

combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

10. (Original) An integrated circuit netlist generation apparatus, comprising:

means for generating a first schematic of an integrated circuit having a plurality of cells therein;

means for generating a second schematic that defines pre-layout electrical interconnects between the plurality of cells of the integrated circuit and approximates parasitic resistances and parasitic capacitances of the pre-layout interconnects; and

means for combining the first and second schematics at corresponding first and second ports within the first and second schematics, respectively.

Claims 11-38 (Canceled).